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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/717,143 | 11/22/2000 | Akihiko Harada | 001545 | 2927 |

23850 7590 12/19/2001

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| EXAMINER | |
|---|---|
| SEFER, AHMED N | |
| **ART UNIT** | **PAPER NUMBER** |
| 2826 | |

DATE MAILED: 12/19/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/717,143 | HARADA ET AL. | |
| | Examiner | Art Unit | |
| | A. Sefer | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *6-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I in Paper No. 5 is acknowledged.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al. US Patent No. 5,610,430.

Yamashita et al disclose (see figs. 1-3 and col. 11, lines 36-52) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate 31 by a substrate isolation insulating

film (unnumbered), provided with a T-shaped gate electrode 13 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern (unnumbered) and having a thickness of the gate insulating film 12 directly under the crosspiece-shaped conductor pattern greater than the thickness of the gate insulting film directly under the main gate electrode.

4. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Imai et al. (JP 8-125187)

Han et al disclose (see fig. 1) an insulated gate type semiconductor device comprised of a semiconductor layer 16 serving as an active region isolated from a semiconductor substrate 14 by a substrate isolation insulating film 15, wherein a thickness of an insulating film provided on a surface of a first conductivity type semiconductor region 9 positioned at an interface between that first conductivity type body contact region 8 and a second conductivity type source 6 and drain 7 regions is made greater than the thickness of a gate insulting film directly under the main gate electrode 5.

5. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Imai et al. (JP 8-125187)

Han et al disclose (see fig. 1) an insulated gate type semiconductor device comprised of a semiconductor layer 16 serving as an active region isolated from a semiconductor substrate 14 by a substrate isolation insulating film 15, wherein a buried insulating film 18 thicker than the thickness of the gate insulting film directly under a gate electrode 5 is provided on a surface of a first conductivity type semiconductor

region 9 positioned at an interface between that first conductivity type body contact region 8 and a second conductivity type source 6 and drain 7 regions.

6. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Kawanaka US Patent No. 5,973,364.

Kawanaka discloses (see fig. 1) an insulated gate type semiconductor device comprised of a semiconductor layer 316 serving as an active region isolated from a semiconductor substrate 312 by a substrate isolation insulating film 314, wherein a gate electrode of an asymmetric T-shape 334 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern is provided and a body contact region 328 and one of a source region 324 and a drain region 326 are isolated through said crosspiece-shaped conductor pattern.

7. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated Yamashita et al. US Patent No. 5,610,430.

Yamashita et al disclose (see figs. 1-3 and col. 11, lines 36-52) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate 31 by a substrate isolation insulating film (unnumbered), wherein a gate electrode of an asymmetric T-shape 13 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern (unnumbered) is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode.

8. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated Yu US Pub. No. 2001/00381123.

Yamashita et al disclose (see figs. 1 and page 2, par. 0022) an insulated gate type semiconductor device comprised of a semiconductor layer serving as an active region isolated from a semiconductor substrate 14 by a substrate isolation insulating film (unnumbered), wherein a gate electrode of an asymmetric T-shape 46 comprised of a trunk-shaped main gate electrode and a crosspiece-shaped conductor pattern (unnumbered) is provided and at least part of said crosspiece-shaped conductor pattern function as a gate electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
December 15, 2001

Nathan Flynn
Primary Examiner